Department of Electronics & Communication Engineering

MINUTES OF 1st MEETING OF BOARD OF STUDIES (BOS)

Date: 06-10-2023

➢ Composition of Board of Studies:

The following members are drafted as members to Board of Studies for the department of Electronics and Communication Engineering

S. No.	BOS Member	Name and Designation of Member
I	Chairperson	Mr. M. Hari Krishna, Professor & HoD
II	Faculty Members :	
	1.	Mr. M. Hari Krishna, Professor & HoD
	2.	Dr. M. Ranga Rao, Professor
	3.	Dr. B. Chandran Mahesh, Professor
	4.	Dr. A. Shravan Kumar, Professor
	5.	Dr. S. Ram Gopal, Professor
	6.	Mr. K. Venkanna, Assoc. Professor
	7.	Mr. Ch. Kutumba Rao, Assoc. Professor
	8.	Mrs. M. Sree Devi, Asst. Professor
	9.	Mr. P. Venkata Krishna, Asst. Professor
	10.	Mr. K. Ravi Babu, Assoc. Professor
	11.	Mr. K. Veera Swami, Asst. Professor
	12	Mrs. P. Dhana Laxmi, Asst. Professor
	13.	Mrs. D. Uma Maheswari, Asst. Professor
	14.	Mr. M. Gopi, Asst. Professor
	15.	Mrs. A, Sirisha, Asst. Professor
	16.	Mrs. Akhila Begum, Asst. Professor
	17.	Mrs.K. Ramya, Asst. Professor
	18.	Mrs. K. Deepthi, Asst. Professor
	19.	Mr. M. Nagendra Babu, Asst. Professor
	20.	Mr. K. Venkateswarlu, Asst. Professor
	21.	Mrs. Y. Padma, Asst. Professor
III	Subject Experts (Academic) :	
	1.	Dr. P. Sreehari Rao, Professor, ECE Dept., National Institute of Technology (NIT), Warangal , TS 8332969357, patri@nitw.ac.in
	2.	Dr. S. Naga Kishore Bhavanam, Professor, ECE Dept., Acharya Nagarjuna University (ANU) Mangalagiri, AP 9989541444, kishore.ece.anu@gmail.com
IV	University Nominee :	Dr. A. Mallikarjuna Prasad, Professor, JNTUK, Kakinada, AP 9441564840, a_malli65@jntucek.ac.in
V	Subject Expert (Industry)	Mr. V. Govinda Rao, Managing Director, Micro Link Information Technologies, Vijayawada, Cell: 9246400662, vgr.mlit@gmail.com
VI	Alumni	Mr. V. Jeevan Kumar (17MG5A0414), System Engineer in Tata Consultancy Services (TCS) at Hyderabad. Contact; 9133607520, jeeva6128@gmail.com
VII	Expert (Outside)	Mr. V. Krishna Rao, SDE, BSNL, Vijayawada Contact: 9490143855, krishnarao.jto@gmail.com

Mr. M. Hari Krishna, Head of the Department, Electronics & Communication Engineering, Sree Vahini Institute of Science and Technology, Tiruvuru chaired the meeting. He expressed his sincere thanks to the entire BoS Members Team for their consent to be on the Board of Studies of the department and their valuable suggestions for improvement. He extended a warm and hearty welcome to all the Hon'ble members of the Board of Studies.

He acknowledged all the members for their valuable suggestions, advice, guidelines and concern towards overall development of the department. Later, he presented the credentials of the college and agenda of the meeting.

Hon'ble BoS Members Dr. A. Mallikarjuna Prasad, Dr. P. Sreehari Rao, Dr. S. Naga Kishore Bhavanam, Mr. V. Govinda Rao, Mr. V. Krishna Rao, Mr. V. Jeevan Kumar have given suggestions and guidelines for the function of Board of Studies.

Functions of the Board of Studies

- Preparation of syllabus for various courses keeping in view of the objectives of the department, interest of the stakeholders for consideration and approval of the Academic Council.
- Suggest methodologies for innovative teaching and evaluation techniques.
- Suggest panel of names to the Academic Council for appointment of examiners.
- Coordinate research, teaching, extension and other academic activities in the department.

With reference to each agenda item, proceedings of Board of studies meeting given below:

Approval of B.Tech ECE- Course Structure & Syllabus of I B.Tech I & II Sem

BOS Chairman informed the details related to the R23 course structure, Syllabus I B.Tech I Sem & II Sem R23 regulations to all the BOS members. As part of the implementation of NEP-2020 across the State of Andhra Pradesh, APSCHE & JNTUK, Kakinada proposed common regulation, course structure and syllabus for all autonomous colleges and affiliated institutions.

The autonomous college may enhance 20% of the syllabus based on the approval from BOS members. The course outcomes may be modified based on the content.

B.Tech. – I Year I Semester (for Group-B Branches- **ECE,** AIML, EEE, ME & Civil)

S. No.	Category	Title	L/D	T	P	Credits
1	BS&H	Engineering Physics	3	0	0	3
2	BS&H	Linear Algebra & Calculus	3	0	0	3
3	Engineering Science	**Basic Electrical & Electronics Engineering**	3	0	0	3
4	Engineering Science	Engineering Graphics	1	0	4	3
5	Engineering Science	Introduction to Programming	3	0	0	3
6	Engineering Science	IT Workshop	0	0	2	1
7	BS&H	Engineering Physics Lab	0	0	2	1
8	Engineering Science	**Electrical & Electronics EngineeringWorkshop**	0	0	3	1.5
9	Engineering Science	Computer Programming Lab	0	0	3	1.5
10	BS&H	NSS/NCC/Scouts & Guides/Community Service	-	-	1	0.5
Total			**13**	**00**	**15**	**20.5**

B.Tech. – I Year II Semester (for Group-B Branches- **ECE,** AIML, EEE, ME & Civil)

S. No.	Category	Title	L	T	P	Credits
1	BS&H	Communicative English	2	0	0	2
2	BS & H	Engineering Chemistry / Chemistry / Fundamental Chemistry	3	0	0	3
3	Engineering Science	Differential Equations & Vector Calculus	3	0	0	3
4	Engineering Science	Basic Civil & Mechanical Engineering	3	0	0	3
5	Professional Core	**Network Analysis**	3	0	0	3
6	BS&H	Communicative English Lab	0	0	2	1
7	BS&H	Engineering Chemistry / Chemistry / Fundamental Chemistry Lab	0	0	2	1
8	Engineering Science	Engineering Workshop	0	0	3	1.5
9	Professional Core	**Network Analysis & Simulation Lab**	0	0	3	1.5
10	BS&H	Health and wellness, Yoga and Sports	-	-	1	0.5
Total			**14**	**00**	**11**	**19.5**

Decision: Noted and approved the course structure and Syllabus.

1. **Approval of B.Tech ECE-Course outcomes of I B.Tech I & II Sem.**

   The BOS chairman informed the course outcomes of I sem & II sem courses and articulation matrix to all the BOS members.

Decision:

Noted and approved the course outcomes specifications and articulation matrix.

2. **Approval of M.Tech VLSI, VLSI&ES - Course Structure & Syllabus of I M. Tech I & II sem and Information on R23 Regulations- P.G (M.Tech).**

   BOS Chairman informed the details related to the R23 course structure, Syllabus I M.Tech I & II sem R23 regulations to all the BOS members.

I M.Tech (VLSI) I Semester (Total Credits: 18)

S.No	Course No	Course Name	L	T	P	Credits
1	PC	CMOS Analog IC Design	3	0	0	3
2	PC	CMOS Digital IC design	3	0	0	3
3	PE	1. VLSI Technology 2. Nanomaterials and Nanotechnology 3. MEMS Technology	3	0	0	3
4	PE	1. Device Modeling 2.Nano-electronics 3.Photonics	3	0	0	3
5		Research methodology and IPR	2	0	0	2
6	Lab 1	CMOS Analog IC Design Lab	0	0	4	2
7	Lab 2	CMOS Digital IC Design Lab	0	0	4	2
8	Aud 1	Audit course-1	2	0	0	0
18						

I M.Tech (VLSI) II Semester (Total Credits: 18)

S.No	Course No	Course Name	L	T	P	Credits
1	PC	Mixed Signal & RF IC Design	3	0	0	3
2	PC	Physical Design Automation	3	0	0	3
3	PE	1. Design For Testability 2. IOT & its Applications 3. VLSI Signal Processing	3	0	0	3
4	PE	1.Network Security & Cryptography 2.Microcontrollers & programmable Digital Signal Processors 3. Low Power VLSI Design	3	0	0	3
5	Lab 1	Mixed Signal IC Design Lab	0	0	4	2
6	Lab 2	Physical Design Automation Lab	0	0	4	2
7	MP	Mini Project	0	0	4	2
8	Aud 2	Audit Course – 2	2	0	0	0
18						

*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

Audit Course 1 & 2

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development through Life Enlightenment Skills

I M.Tech (VLSI & ES) I Semester (Total Credits: 18)

S.No	Course No	Course Name	L	T	P	Credits
1	PC	RTL Simulation and Synthesis with PLDs	3	0	0	3
2	PC	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
3	PE	1. Digital Signal and Image Processing 2. Parallel Processing 3. VLSI signal processing	3	0	0	3
4	PE	1. Programming Languages for Embedded Systems 2. System Design with Embedded Linux3.CAD of Digital System	3	0	0	3
5		Research methodology and IPR	2	0	0	2
6	Lab 1	RTL Simulation and Synthesis with PLDs Lab	0	0	4	2
7	Lab 2	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	2
8	Aud 1	Audit course-1	2	0	0	0
18						

I M.Tech (VLSI & ES) II Semester (Total Credits: 18)

S.No	Course No	Course Name	L	T	P	Credits
1	PC	Analog and Digital CMOS VLSI Design	3	0	0	3
2	PC	Real Time Operating Systems	3	0	0	3
3	PE	1. Memory Architectures 2. SoC Design 3. Low power VLSI Design	3	0	0	3
4	PE	1. Communication Buses and Interfaces 2. Network Security and Cryptography 3. Physical design automation	3	0	0	3
5	Lab 1	Analog and Digital CMOS VLSI Design Lab	0	0	4	2
6	Lab 2	Real Time Operating Systems Lab	0	0	4	2
7	MP	Mini Project	0	0	4	2
8	Aud 2	Audit Course – 2	2	0	0	0
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*Students be encouraged to go to Industrial Training/Internship for at least 2-3 weeks during semester break.

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3. Approval of M.Tech (VLSI, VLSI&ES)-Course outcomes of I M.Tech I & II Sem.

The BOS chairman informed the course outcomes of I sem & II sem courses and articulation matrix to all the BOS members.

Decision:

Noted and approved the course outcomes specifications and articulation matrix.

4. Any other matter with permission of Chair.

- BOS chairman is informed to prepare the proposed calendar of events organized for students and faculty for the A. Y. 2023-24.

Decision: Noted

1st MEETING OF BOARD OF STUDIES

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	2.	Dr. S. Naga Kishore Bhavanam, Professor, ECE Dept., Acharya Nagarjuna University (ANU) Mangalagiri, AP 9989541444, kishore.ece.anu@gmail.com	Online
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VII	**Expert (Outside)**	Mr. V. Krishna Rao, SDE, BSNL, Vijayawada Contact: 9490143855, krishnarao.jto@gmail.com	Online

Date: 31/10/23

BOS Chairperson

Head of the Department
Electronics and Communication Engineering
Sree Vahini Institute of Science & Technology
TIRUVURU, Krishna Dt. Pin-521 235